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EXAMINER	
MCGUE, FRANK J	

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3662	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/570,833	UNDERBRINK ET AL.	
	Examiner	Art Unit	
	FRANK MCGUE	3662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/22/2006, 09/10/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Inventorship

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Specification

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

The term "significantly greater" in claims 24, 26, 28 and 30 is a relative term which renders the claim indefinite. The term "significantly" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and

one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Appropriate correction is required.

The term "optimal pattern" in claims 12, 37 and 47 is a relative term which renders the claim indefinite. The term "optimal" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Appropriate correction is required.

The terms "wide, low resolution" and “narrow, high resolution” in claims 21 and 40 are relative terms which renders the claim indefinite. The term "optimal" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 9-15, 17-18, 31, 43, 46-49 and 51 are rejected under 35 U.S.C. 102(b) as being anticipated by Rabenko et al. (US Pat 6765931).

With regard to claim 1, Rabenko et al. have an electronic system (network gateway, Abstract) with at least one processor 160 (col. 9, lines 31-35) with a signal

processing system DSP 600 coupled to the processor 160 (col. 36, line 65 – col. 37, line 4). The signal processing system operates in accordance with operational modes of the system (col. 45, lines 58-61). The signal processing system DSP 600 includes an input sample subsystem 736 that receives data via at least one channel and produces input data samples (col. 44, lines 45-47). The signal processing system DSP 600 further includes a signal processing subsystem coupled to the processor 160 which includes at least one matched filter having at least one configurable parameter automatically configured in accordance with the operational modes (col. 9, lines 43-45; col. 46, line 60 – col. 47, line 2; col. 47, lines 20-32). The signal processing system further includes an FFT subsystem coupled to the processor 160 that has at least one of a number of inputs and a transform size automatically configured in accordance with the operational modes (col. 63, lines 33-35) and a memory subsystem automatically configurable into a plurality of configurations according to the operational modes (col. 44, lines 52-53).

With regard to claim 2, Rabenko et al. automatically scales gain in response to a level of the received data (col. 59, line 41).

With regard to claim 3, Rabenko et al. have the input sample subsystem automatically control decimation of the received data in accordance with the operational modes (col. 83, lines 55-60).

With regard to claim 4, Rabenko et al. control decimation including at least one decimation mode selected according to an amount of memory consumed (data overflow) and at least a second decimation mode selected according to the amount of received data (data underflow) (col. 29, lines 40-58).

With regard to claim 8, Rabenko et al. have the memory subsystem configured into regions (partitions) each being accessed by a plurality of manners (descriptors) (partitions, col. 13, lines 6-9) wherein each region is accessed by particular subsystems (col. 13, lines 19-23) wherein one of the regions stores data words from the processor that determines the configuration of the memory subsystem including sizes of the regions and manners of access (col. 13, lines 15-18).

With regard to claim 9, Rabenko et al. further describe at least one sequencer (DOSCIS) coupled to the processor that automatically controls time multiplexed use of at least one of the input sample subsystem, signal processing subsystem and the FFT subsystem (col. 6, lines 52-62; col. 17, lines 30-48).

With regard to claim 10, Rabenko et al. further describe the sequencer (DOSCIS) controlling data by controlling channel access to at least one of the input sample subsystem, signal processing subsystem and the FFT subsystem (col. 6, lines 52-62; col. 17, lines 30-48).

With regard to claim 11, Rabenko et al. automatically configure at least one of the signal processing subsystem and the FFT subsystem using information from the memory subsystem (col. 18, line 62- col. 19, line 12).

With regard to claim 12, Rabenko et al. has a first controller 150 that controls storage of data from the signal processing subsystem using an optimal pattern which allows simultaneous access by the FFT subsystem while avoiding collisions among the accessed data (col. 13, lines 9-12).

With regard to claim 13, Rabenko et al. further comprise at least one second controller 150 coupled among the input sample subsystem and the signal processing subsystem to control access to the memory subsystem (col. 12, lines 38-60).

With regard to claim 14, Rabenko et al. further comprise at least one third controller 112 coupled among the signal processing subsystem, the FFT subsystem and the memory subsystem (col. 10, lines 38-65).

With regard to claim 15, in Rabenko et al. the third controller 116 controls transfer of data among the signal processing system and the FFT subsystem (col. 10, lines 38-65).

With regard to claim 17, Rabenko et al. provide that the memory subsystem comprises a first memory area 114 coupled for access by a first processor 128 via a first bus 118 and a second memory area 114 (partitions) coupled for access by a second processor 150 via a second bus 186 having configurations allowing each of the processors access to data in the other memory area (col. 13, lines 6-37).

With regard to claim 18, Rabenko et al. have two receivers each with a clock (ADC & TRC) each of which generate first and second clock signals which generate values which are stored and a ratio counter (sampling rate tracker) which generates a control signal 554(b) and counts pulses 557(a), 557(b) of the first and second clock signals and captures the count of each clock signal (see Fig. 18a) and then determines a ratio between frequencies of the first and second clock signals using the count (col. 30, lines 11-36).

With regard to claim 31, Rabenko et al. is an electronic system which includes one of cellular telephones, portable telephones, portable communications devices, personal computers, portable computing devices and personal digital assistants (abstract).

With regard to claim 43, Rabenko et al. have an electronic system (network gateway, Abstract) comprising at least one processor 160 (col. 9, lines 31-35) and a signal processor DSP 600 operating according to a plurality of operational modes (col. 45, lines 58-61). The signal processor DSP 600 includes a signal processing subsystem that is automatically and dynamically configurable in response with the operational modes (col. 9, lines 43-45; col. 46, line 60 – col. 47, line 2; col. 47, lines 20-32). The signal processor further includes an FFT subsystem that is automatically and dynamically configurable in response to the operational modes (col. 63, lines 33-35). The signal processor DSP 600 further includes a memory subsystem automatically and dynamically configurable in response to the operational modes (col. 44, lines 52-53). Rabenko et al. has a first controller 116 that controls transfer of data among the signal processing system and the FFT subsystem (col. 10, lines 38-65). Rabenko et al. have configurability of the memory subsystem includes configuring the memory subsystem into regions (partitions) according to operational modes, each region being accessed by a plurality of manners (descriptors) according to the operational modes (partitions, col. 13, lines 6-9).

With regard to claim 46, Rabenko et al. have at least one of the regions stores data words from the processor that determines the configuration of the memory subsystem including sizes of the regions and manners of access (col. 13, lines 15-18).

With regard to claim 47, Rabenko et al. has a second controller 150 that controls storage of data from the signal processing subsystem using an optimal pattern which allows simultaneous access to data by the FFT subsystem while avoiding collisions among the accessed data (col. 13, lines 9-12).

With regard to claim 48, Rabenko et al. is an electronic system which includes one of cellular telephones, portable communications devices and portable computing devices (abstract).

With regard to claim 49, Rabenko et al. recites a serial interface between the signal processing system and the input sample system (col. 13, lines 38-55).

With regard to claim 51, Rabenko et al. have an electronic system (network gateway, Abstract) comprising means for controlling processing 160 (col. 9, lines 31-35) and means for processing signals DSP 600 coupled to the means for controlling processing 160 (col. 36, line 65 – col. 37, line 4). The means for processing signals operates in accordance with operational modes of the system (col. 45, lines 58-61). The means for processing DSP 600 includes means for receiving data and producing input data samples 736 that receives data via at least one channel and produces input data samples (col. 44, lines 45-47). Means for generating coherent data using the input data samples includes at least one matched filter means having at least one configurable parameter automatically configured in accordance with the operational

modes (col. 9, lines 43-45; col. 46, line 60 – col. 47, line 2; col. 47, lines 20-32). Means for generating FFTs has a number of inputs and a transform size automatically configured in accordance with the operational modes (col. 63, lines 33-35). Means for storing data is automatically configurable into a plurality of configurations according to the operational modes (col. 44, lines 52-53).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al. as applied to claim 1 further in view of Kanack et al. (US Pat 6263034).

With regard to claim 5, Rabenko et al. have the at least one configurable parameter of the matched filter being the number of taps (col. 66, lines 55-62) as does Kanack et al. which also shows the number of accumulations and a tap offset (col. 8, line 44 - col. 9, line 2). It would have been obvious to modify Rabenko et al. by adding the filter control parameters of Kanack et al. in order to reduce “jitter” in a digital processing system.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al. as applied to claim 1 further in view of Coleman et al. (US Pat 3939474).

With regard to claim 6, Coleman et al. show that it is long known to use coherent data in signal processing (col. 2, line 67- col. 3, line 1). It would have been obvious to modify Rabenko et al. by using coherent data as taught in Coleman et al. in order to improve CNR and extended signal range performance.

Claim 7, 16, 19-20 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al. as applied to claim 1 further in view of Sih et al. (US Pat 6480529).

With regard to claim 7, Sih et al. teach feeding the output of a matched filter to a coherent accumulator (col. 4, lines 1-10). It would have been obvious to modify Rabenko et al. to provide the matched filter output to a coherent accumulator in order to provide a fast and flexible and efficient system.

With regard to claim 16, Sih et al. teach feeding data from an FFT system to a non-coherent accumulator (col. 4, lines 11-14). It would have been obvious to modify Rabenko et al. to provide a non-coherent accumulator in order to provide a fast and flexible and efficient system.

With regard to claim 19, Sih et al. teaches a signal processing system being configurable to process satellite signal data in a satellite based positioning system (Abstract). It would have been obvious to modify Rabenko et al. to handle a satellite system as taught in Sih et al. in order to provide high performance and robust operation to a positioning system.

With regard to claim 20, Sih et al. teach the ability to use both the IS-95 system and a GPS system (Abstract). It would have been obvious to modify Rabenko et al. to handle a both satellite system and a terrestrial system as taught in Sih et al. in order to provide positioning service using two sources for robust operation.

With regard to claim 23, the memory subsystem of Rabenko et al. is configurable into regions that include an input sample memory (Rabenko et al., col. 13, lines 19-37) while Sih et al. teach storage of coherent data in a coherent memory (Sih et al., col. 4, lines 1-3) and an incoherent summation that stores incoherent data (col. 4, lines 11-12). It would have been obvious to modify Rabenko et al. as applied to claim 1 by configuring the memory into regions as taught in both Rabenko et al. and Sih et al. to store input samples, coherent data and incoherent data in order to provide an organizational structure to said data and samples.

Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al. as applied to claim 1 further in view of Schuchman et al. (US Pat 5365450).

With regard to claim 21, Schuchman et al. show that it has long been known that GPS includes operational modes including a wide, low resolution search (cold start, col. 1, lines 41-58), a narrow, high precision search (hot start, col. 2, lines 8-28) and a tracking mode (col. 2, lines 29-41). It would have been obvious to modify Rabenko et al. by using Schuchman's operational modes in order to provide an operational framework for position determination.

With regard to claim 22, Schuchman et al. show that it has long been known that GPS includes operational modes including a cold start (col. 1, lines 41-58), a coarse acquisition mode (warm start, col. 1, line 59 – col. 2, line 7), a hot start (col. 2, lines 8-28) and a tracking mode (col. 2, lines 29-41). It would have been obvious to modify Rabenko et al. by using Schuchman's operational modes in order to provide an operational framework for position determination.

Claims 24, 26, 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al. as applied to claim 1 further in view of Schuchman et al. and Sih et al.

With regard to claim 24, Schuchman et al. show that it has long been known that GPS includes operational modes including a cold start (col. 1, lines 41-58). Rabenko et al. have the memory subsystem configured into regions (partitions, col. 13, lines 6-9) that include an input sample memory (Rabenko et al., col. 13, lines 19-37) while Sih et al. teach storage in incoherent summation (NCS memory) that stores incoherent data (col. 4, lines 11-12). In Rabenko et al., the input sample memory is filled with input data samples in a one-shot manner such that the signal processing subsystem processes data in the filled input sample memory at least once before the data is overwritten (Rabenko et al., Fig. 4, col. 13, lines 6-27). It would have been obvious to modify Rabenko et al. as applied to claim 1 by using the operational modes of Schuchman et al. and configuring the memory into regions as taught in both Rabenko et al. and Sih et

al. to store input samples and incoherent data in order to provide an organizational structure to said data and samples.

With regard to claim 26, Schuchman et al. show that it has been long known to provide a coarse acquisition mode (warm start, col. 1, line 59 – col. 2, line 7), Rabenko et al. have the memory subsystem configured into regions (partitions, col. 13, lines 6-9) that include an input sample memory (Rabenko et al., col. 13, lines 19-37) while Sih et al. teach storage of coherent data in a coherent memory (Sih et al., col. 4, lines 1-3) and an incoherent summation that stores incoherent data (col. 4, lines 11-12). In Rabenko et al., the input sample memory is filled with input data samples in a cyclic manner such that the signal processing subsystem reads out data from one area while the input sample subsystem writes data to another area (Rabenko et al., Fig. 4, col. 13, lines 6-27). It would have been obvious to modify Rabenko et al. as applied to claim 1 by using the operational modes of Schuchman et al. and configuring the memory into regions as taught in both Rabenko et al. and Sih et al. to store input samples, coherent data and incoherent data in order to provide an organizational structure to said data and samples.

With regard to claim 28, Schuchman et al. show that it has been long known to provide a hot start (col. 2, lines 8-28), Rabenko et al. have the memory subsystem configured into regions (partitions, col. 13, lines 6-9) that include an input sample memory (Rabenko et al., col. 13, lines 19-37) while Sih et al. teach storage of coherent data in a coherent memory (Sih et al., col. 4, lines 1-3) and an NCS memory that stores incoherent data (Sih et al., col. 4, lines 11-12). In Rabenko et al., the input sample memory is filled with input data samples in a cyclic manner such that the signal

processing subsystem reads out data from one area while the input sample subsystem writes data to another area (Rabenko et al., Fig. 4, col. 13, lines 6-27). In Sih et al. the signal processing unit produces coherent data which is stored in the coherent memory (col. 5, lines 52-54) which is configured to include a scratch area and a plurality of coherent areas, each for storage of coherent data from a satellite (Sih et al., 5, lines 52-62). It would have been obvious to modify Rabenko et al. as applied to claim 1 by using the operational modes of Schuchman et al. and configuring the memory into regions as taught in both Rabenko et al. and Sih et al. to store input samples, coherent data and incoherent data in order to provide an organizational structure to said data and samples.

With regard to claim 30, Schuchman et al. show that it has been long known to provide a tracking mode (col. 2, lines 29-41), Rabenko et al. have the memory subsystem configured into regions (partitions, col. 13, lines 6-9) that include an input sample memory (Rabenko et al., col. 13, lines 19-37) while Sih et al. teach storage of coherent data in a coherent memory (Sih et al., col. 4, lines 1-3) and an NCS memory that stores incoherent data (Sih et al., col. 4, lines 11-12). In Rabenko et al., the input sample memory is filled with input data samples in a cyclic manner such that the signal processing subsystem reads out data from one area while the input sample subsystem writes data to another area (Rabenko et al., Fig. 4, col. 13, lines 6-27). In Sih et al. the signal processing unit produces coherent data which is stored in the coherent memory (col. 5, lines 52-54) which is configured to include a scratch area and a plurality of coherent areas, each for storage of coherent data from a satellite (Sih et al., 5, lines 52-62). The coherent data is read to a subsystem which, in Rabenko et al., can be an FFT

subsystem (Rabenko et al., col. 63, lines 33-35). The FFT subsystem produces noncoherent data and stores same in the NCS memory (non-coherent accumulator) (Sih et al., col. 7, lines 1-13). Rabenko et al. have a memory subsystem such as the NCS memory configured into regions (partitions, col. 13, lines 6-9). It would have been obvious to modify Rabenko et al. as applied to claim 1 by using the operational modes of Schuchman et al. and by configuring the memory into regions as taught in both Rabenko et al.,and Sih et al. to store input samples, coherent data and incoherent data in order to provide an organizational structure to said data and samples.

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al., Schuchman et al. and Sih et al as applied to claim 24 further in view of Sih et al. and Rabenko et al. In Sih et al. the signal processing unit produces coherent data which is transmitted to a subsystem (col. 5, lines 52-54) which, in Rabenko et al., can be an FFT subsystem (Rabenko et al., col. 63, lines 33-35) which produces noncoherent data and stores same in the NCS memory (non-coherent accumulator) (Sih et al., col. 7, lines 1-13). It would have been obvious to modify Rabenko et al., Sih et al. and Schuchman et al. as applied to claim 24 by directing coherent and incoherent data to two locations in order to avoid mathematical conundrums by improper usage of same.

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al., Schuchman et al. and Sih et al as applied to claim 26 further in view of Sih et al. and Rabenko et al. In Sih et al. the signal processing unit produces coherent data which is stored in the coherent memory (col. 5, lines 52-54) which is moved to a subsystem which, in Rabenko et al., can be an FFT subsystem (Rabenko et al., col. 63, lines 33-35). It would have been obvious to modify Rabenko et al., Sih et al. and Schuchman et al. as applied to claim 26 by directing coherent data to coherent memory and FFT in order to provide the proper data to a coherent process.

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al., Schuchman et al. and Sih et al as applied to claim 28 further in view of Sih et al. and Rabenko et al. In Sih et al. the signal processing unit produces coherent data which is stored in the coherent memory (col. 5, lines 52-54) which is moved to a subsystem which, in Rabenko et al., can be an FFT subsystem (Rabenko et al., col. 63, lines 33-35). It would have been obvious to modify Rabenko et al., Sih et al. and Schuchman et al. as applied to claim 28 by directing coherent data to coherent memory and FFT in order to provide the proper data to a coherent process.

Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al. further in view of Williams (US Pat 6344749).

With regard to claim 32, Rabenko et al. have an electronic system (network gateway, Abstract) comprising at least one processor 160 (col. 9, lines 31-35) and a

signal processing system DSP 600 coupled to operate under a plurality of operational modes (col. 45, lines 58-61). The signal processing system DSP 600 includes a signal processing subsystem that is automatically and dynamically configurable in response with the operational modes (col. 9, lines 43-45; col. 46, line 60 – col. 47, line 2; col. 47, lines 20-32). The signal processing system further includes an FFT subsystem that is automatically and dynamically configurable in response to the operational modes (col. 63, lines 33-35). The signal processing subsystem further includes at least one matched filter having at least one configurable parameter automatically configured in accordance with the operational modes (col. 9, lines 43-45; col. 46, line 60 – col. 47, line 2; col. 47, lines 20-32). Williams teaches that it is well known that FFT subsystems have at least one of a number of inputs (col. 9, lines 28-31) and the transform size is automatically configured in accordance with operational modes (col. 9, lines 42-45). It would have been obvious to modify Rabenko et al. by using the automatically configured FFT transform as taught in Williams in order to take advantage of the properties of this well known mathematical technique.

Claims 33-34, 36-38 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al. and Williams as applied to claim 32 further in view of Rabenko et al.

With regard to claim 33, in Rabenko et al. the signal processing system DSP 600 includes an input sample subsystem 736 coupled to the processor that receives data via at least one channel and produces input data samples (col. 44, lines 45-47). It would

have been obvious to modify Rabenko et al. and Williams as applied to claim 32 in order to control data input to the system.

With regard to claim 34, Rabenko et al. have a memory subsystem automatically and dynamically configured into a plurality of configurations according to the operational modes wherein the memory subsystem is configurable into regions (partitions) wherein each region stores a type of data and each region is accessible by a plurality of manners (descriptors) (partitions, col. 13, lines 6-9) wherein each region is accessed by particular subsystems (col. 13, lines 19-23) wherein one of the regions stores data words from the processor that determines the configuration of the memory subsystem including sizes of the regions and manners of access (col. 13, lines 15-18). It would have been obvious to modify Rabenko et al. and Williams as applied to claim 32 by using the memory subsystem of Rabenko et al. in order to organize incoming data for use by the other subsystems.

With regard to claim 36, Rabenko et al. further describe at least one sequencer (DOSCIS) coupled to the processor that automatically and dynamically controls time multiplexed use of at least one of the signal processing subsystem and the FFT subsystem (col. 6, lines 52-62; col. 17, lines 30-48) by controlling channel access to at least one of the signal processing subsystem and the FFT subsystem in accordance with at least one rule (col. 6, lines 52-62; col. 17, lines 30-48). In Rabenko et al., the sequencer automatically configures at least one of the signal processing subsystem and the FFT subsystem using information from the at least one memory area (col. 18, line 62- col. 19, line 12). It would have been obvious to modify Rabenko et al. and Williams

as applied to claim 32 by providing a sequencer as taught in Rabenko et al. in order to process data more efficiently.

With regard to claim 37, Rabenko et al. has a first controller 150 that controls storage of data from the signal processing subsystem using an optimal pattern which allows simultaneous access by the FFT subsystem while avoiding collisions among the accessed data (col. 13, lines 9-12). It would have been obvious to modify Rabenko et al. and Williams as applied to claim 32 by providing a first controller in order to control the flow of data within the system.

With regard to claim 38, Rabenko et al. further comprise at least one second controller 112 coupled among the signal processing subsystem, the FFT subsystem and the memory subsystem (col. 10, lines 38-65) which controls transfer of data among the signal processing system and the FFT subsystem (col. 10, lines 38-65). It would have been obvious to modify Rabenko et al. and Williams as applied to claim 32 by providing a second controller in order to control the flow of data within the system.

With regard to claim 42, Rabenko et al. is an electronic system which includes one of cellular telephones, portable telephones, portable communications devices, personal computers, portable computing devices and personal digital assistants (abstract). It would have been obvious to modify Rabenko et al. and Williams as applied to claim 32 by using with various devices in order to provide access to networks for such devices.

Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al. and Williams as applied to claim 32 further in view of Kanack et al. Rabenko et al. have the at least one configurable parameter of the matched filter being the number of taps (col. 66, lines 55-62) as does Kanack et al. which also shows the number of accumulations and a tap offset (col. 8, line 44 - col. 9, line 2). It would have been obvious to modify Rabenko et al. and Williams by adding the filter control parameters of Kanack et al. in order to reduce "jitter" in a digital processing system.

Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al. and Williams as applied to claim 32 further in view of Sih et al. Sih et al. teaches a signal processing system being configurable to process satellite signal data in a satellite based positioning system (Abstract). It would have been obvious to modify Rabenko et al. and Williams as applied to claim 32 to handle a satellite system as taught in Sih et al. in order to provide high performance and robust operation of the present invention to a positioning system.

Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al., Williams and Sih et al. as applied to claim 39 further in view of Schuchman et al. Schuchman et al. show that it has long been known that GPS includes operational modes including a cold start (col. 1, lines 41-58), a hot start (col. 2, lines 8-28) and a tracking mode (col. 2, lines 29-41). It would have been obvious to modify Rabenko et al., Williams and Sih et al. as applied to claim 39 by using

Schuchman's operational modes in order to provide an operational framework for position determination.

Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al. and Williams as applied to claim 32 further in view of Schuchman et al. Schuchman et al. show that it has long been known that GPS includes operational modes including a cold start (col. 1, lines 41-58), a coarse acquisition mode (warm start, col. 1, line 59 – col. 2, line 7), a hot start (col. 2, lines 8-28) and a tracking mode (col. 2, lines 29-41). It would have been obvious to modify Rabenko et al. by using Schuchman's operational modes in order to provide an operational framework for position determination.

Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al. as applied to claim 43 further in view of Williams (US Pat 6344749). In Rabenko et al. the signal processing subsystem further includes at least one matched filter having at least one configurable parameter automatically configured in accordance with the operational modes (col. 9, lines 43-45; col. 46, line 60 – col. 47, line 2; col. 47, lines 20-32). Williams teaches that it is well known that FFT subsystems have at least one of a number of inputs (col. 9, lines 28-31) and the transform size is automatically configured in accordance with operational modes (col. 9, lines 42-45). It would have been obvious to modify Rabenko et al. as applied to claim 43 by using the automatically

configured FFT transform as taught in Williams in order to take advantage of the properties of this well known mathematical technique.

Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al. as applied to claim 43 further in view of Sih et al. and Schuchman et al. In Rebenko et al. the signal processing system DSP 600 includes an input sample subsystem 736 that receives data via at least one channel and produces input data samples (col. 44, lines 45-47). Sih et al. teaches a signal processing system being configurable to process satellite signal data in a satellite based positioning system (Abstract). Schuchman et al. show that it has long been known that GPS includes operational modes including a wide, low resolution search (cold start, col. 1, lines 41-58), a narrow, high precision search (hot start, col. 2, lines 8-28) and a tracking mode (col. 2, lines 29-41). It would have been obvious to modify Rebenko et al. as applied to claim 43 by using the system with GPS as taught in Sih et al. and using the modes of Schuchman et al. in order to provide robust operation to the GPS locating service.

Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al. as applied to claim 1 further in view of Horton (US Pat 6421696). With regard to claim 50, Horton shows that twiddle factors or algorithms are well known techniques used in connection with fast Fourier transforms. It would have obvious to modify Rabenko et al. as applied to claim 1 by using twiddle factors as taught in Horton in order to take advantage of these well known mathematical techniques.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-4, 6, 8-15, 17-19, 31, 43 and 46-49 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of Falk et al. (U.S. Pat 7639180) in view of Rabenko et al.

With regard to claim 1, Falk et al. have an electronic system (Falk et al., col. 20, line 45) with at least one processor (CPU, Falk et al., col. 20, line 46) with a signal processing system (Falk et al., col. 20, line 47) coupled to the processor (Falk et al., col. 20, lines 48-49). The signal processing system operates in accordance with operational modes of the system (Falk et al., col. 20, lines 59-60, see also Rabenko et al., col. 45, lines 58-61). The signal processing system includes an input sample subsystem (Falk et al., col. 20, 50-51) that receives data (Falk et al., col. 20, line 8) via at least one channel (Rabenko et al., col. 44, lines 45-47) and produces input data samples (Falk et al, col. 20, line 53). The signal processing system further includes a signal processing subsystem (Falk et al., col. 20, lines 54-55) coupled to the processor which includes at least one matched filter having at least one configurable parameter automatically configured in accordance with the operational modes (Rabenko et al., col. 9, lines 43-45; col. 46, line 60 – col. 47, line 2; col. 47, lines 20-32). The signal processing system further includes an FFT subsystem (Falk et al., col. 20, lines 55-56) coupled to the processor that has at least one of a number of inputs and a transform

size automatically configured in accordance with the operational modes (Rabenko et al. col. 63, lines 33-35) and a memory subsystem (memory device, Falk et al., col. 20, line 58) automatically configurable into a plurality of configurations according to the operational modes (Rabenko et al., col. 44, lines 52-53). It would have been obvious to modify Falk et al. as provided in Rabenko et al., in order to speed up calculations by organizing the memory subsystem properly.

With regard to claim 2, Rabenko et al. automatically scales gain in response to a level of the received data (col. 59, line 41). It would have been obvious to modify Falk et al. and Rabenko et al. as applied to claim 1 by scaling gain as taught in Rabenko et al. in order to better process different levels of received data.

With regard to claim 3, Rabenko et al. have the input sample subsystem automatically control decimation of the received data in accordance with the operational modes (col. 83, lines 55-60). It would have been obvious to modify Falk et al. and Rabenko et al. as applied to claim 1 by automatically controlling decimation as taught in Rabenko et al. in order to provide better functionality.

With regard to claim 4, Rabenko et al. control decimation including at least one decimation mode selected according to an amount of memory consumed (data overflow) and at least a second decimation mode selected according to the amount of received data (data underflow) (col. 29, lines 40-58). It would have been obvious to modify Falk et al. and Rabenko et al. as applied to claim 3 by selecting decimation by either memory consumed or received data as taught in Rabenko et al. in order to provide better functionality.

With regard to claim 6, Falk et al. show signal processing means generating coherent data (Falk et al., col. 20, lines 54-55). It would have been obvious to modify Rabenko et al. and Falk et al. as applied to claim 1 by using coherent data as taught in Falk et al. in order to improve CNR and extended signal range performance.

With regard to claim 8, Falk et al. and Rabenko et al. have the memory subsystem configured into regions (Falk et al., col. 20, line 17; Rabenko et al., partitions) each being accessed by a plurality of manners (descriptors) (partitions, col. 13, lines 6-9) wherein each region is accessed by particular subsystems (Falk et al, col. 20, lines 18-19; Rabenko et al., col. 13, lines 19-23) wherein one of the regions stores data words from the processor (Falk et al., col. 20, lines 19-20) that determines the configuration of the memory subsystem including sizes of the regions and manners of access (Falk et al., col 20, line 21; Rabenko et al., col. 13, lines 15-18). It would have been obvious to modify Falk et al. and Rabenko et al. as applied to claim 1 by using the memory configuration as taught in both references in order to easily access data.

With regard to claim 9, Rabenko et al. further describe at least one sequencer (DOSCIS) coupled to the processor that automatically controls time multiplexed use of at least one of the input sample subsystem, signal processing subsystem and the FFT subsystem (col. 6, lines 52-62; col. 17, lines 30-48). It would have been obvious to modify Falk et al. and Rabenko et al. as applied to claim 1 by using a sequencer as taught in Rabenko et al. in order to process data more efficiently.

With regard to claim 10, Rabenko et al. further describe the sequencer (DOSCIS) controlling data by controlling channel access to at least one of the input

sample subsystem, signal processing subsystem and the FFT subsystem (col. 6, lines 52-62; col. 17, lines 30-48). It would have been obvious to modify Falk et al. and Rabenko et al. as applied to claim 9 by using the sequencer to control access as taught in Rabenko et al. in order to provide better processing flow in the system.

With regard to claim 11, Rabenko et al. automatically configure at least one of the signal processing subsystem and the FFT subsystem using information from the memory subsystem (col. 18, line 62- col. 19, line 12). It would have been obvious to modify Falk et al. and Rabenko et al. as applied to claim 9 by using the sequencer to configure subsystems as taught in Rabenko et al. in order to provide a more efficient system for operations between the memory and the particular subsystem.

With regard to claim 12, Rabenko et al. has a first controller 150 that controls storage of data from the signal processing subsystem using an optimal pattern which allows simultaneous access by the FFT subsystem while avoiding collisions among the accessed data (col. 13, lines 9-12). It would have been obvious to modify Falk et al. and Rabenko et al. as applied to claim 1 by using a first controller as taught in Rabenko et al. in order to store data more efficiently.

With regard to claim 13, Rabenko et al. further comprise at least one second controller 150 coupled among the input sample subsystem and the signal processing subsystem to control access to the memory subsystem (col. 12, lines 38-60). It would have been obvious to modify Falk et al. and Rabenko et al. as applied to claim 1 by using a second controller as taught in Rabenko et al. in order to control data access more efficiently.

With regard to claim 14, Rabenko et al. further comprise at least one third controller 112 coupled among the signal processing subsystem, the FFT subsystem and the memory subsystem (col. 10, lines 38-65). It would have been obvious to modify Falk et al. and Rabenko et al. as applied to claim 1 by using a third controller as taught in Rabenko et al. in order to transfer data more efficiently between subsystems.

With regard to claim 15, in Rabenko et al. the third controller 116 controls transfer of data among the signal processing system and the FFT subsystem (col. 10, lines 38-65). It would have been obvious to modify Falk et al. and Rabenko et al. as applied to claim 14 by using the third controller as taught in Rabenko et al. in order to control data transfer more efficiently between the signal processing subsystem and the FFT subsystem.

With regard to claim 17, Rabenko et al. provide that the memory subsystem comprises a first memory area 114 coupled for access by a first processor 128 via a first bus 118 and a second memory area 114 (partitions) coupled for access by a second processor 150 via a second bus 186 having configurations allowing each of the processors access to data in the other memory area (col. 13, lines 6-37). It would have been obvious to modify Falk et al. and Rabenko et al. as applied to claim 1 by using buses as taught in Rabenko et al. in order to transfer data using this well known technology.

With regard to claim 18, Rabenko et al. have two receivers each with a clock (ADC & TRC) each of which generate first and second clock signals which generate values which are stored and a ratio counter (sampling rate tracker) which generates a

control signal 554(b) and counts pulses 557(a), 557(b) of the first and second clock signals and captures the count of each clock signal (see Fig. 18a) and then determines a ratio between frequencies of the first and second clock signals using the count (col. 30, lines 11-36). It would have been obvious to modify Falk et al. and Rabenko et al. as applied to claim 1 by clocks and counters as taught in Rabenko et al. in order to provide an internal clock for comparison with incoming GPS data.

With regard to claim 19, Falk et al. teach a signal processing system being configurable to process satellite signal data in a satellite based positioning system (Falk et al., col. 20, lines 47-48). It would have been obvious to modify Rabenko et al. and Falk et al. as applied to claim 1 to handle a satellite system as taught in Falk et al. in order to provide high performance and robust operation to a positioning system.

With regard to claim 31, Rabenko et al. is an electronic system which includes one of cellular telephones, portable telephones, portable communications devices, personal computers, portable computing devices and personal digital assistants (abstract). It would have been obvious to modify Falk et al. and Rabenko et al. as applied to claim 1 by use with the suggested devices of Rabenko et al. in order to provide a platform for the present invention.

With regard to claim 43, Falk et al. and Rabenko et al. have an electronic system (Falk et al., col. 20, line 45; Rabenko et al., network gateway, Abstract) comprising at least one processor (CPU, Falk et al., col. 20, line 46; Rabenko et al., col. 9, lines 31-35) and a signal processor (signal processing system, Falk et al., col. 20, line 47) operating according to a plurality of operational modes (Rabenko et al., col. 45, lines 58-

61). The signal processor includes a signal processing subsystem (Falk et al., col. 20, lines54-55) that is automatically and dynamically configurable in response with the operational modes (Rabenko et al., col. 9, lines 43-45; col. 46, line 60 – col. 47, line 2; col. 47, lines 20-32). The signal processor further includes an FFT subsystem (Falk et al., col. 20, lines 55-56) that is automatically and dynamically configurable in response to the operational modes (Rabenko et al., col. 63, lines 33-35). The signal processor further includes a memory subsystem (memory device, Falk et al., col. 20, line 58) automatically and dynamically configurable in response to the operational modes (Falk et al., col. 20, lines 58-60; Rabenko et al., col. 44, lines 52-53). Rabenko et al. has a first controller 116 that controls transfer of data among the signal processing system and the FFT subsystem (col. 10, lines 38-65). The configurability of the memory subsystem includes configuring the memory subsystem into regions (partitions) according to operational modes, each region being accessed by a plurality of manners (descriptors) according to the operational modes (Falk et al., col. 20, lines 61-65; Rabenko et al., partitions, col. 13, lines 6-9). It would have been obvious to modify Falk et al. as taught in Rabenko et al. in order to speed up calculations by organizing the memory subsystem to operate efficiently under different conditions.

With regard to claim 46, both Falk et al., and Rabenko et al. have at least one of the regions stores data words from the processor that determines the configuration of the memory subsystem including sizes of the regions and manners of access (Falk et al., col. 20, lines 63-65; Rabenko et al., col. 13, lines 15-18). It would have been

obvious to modify Falk et al. and Rabenko et al. as applied to claim 43 by using the memory configuration as taught in both references in order to easily access data.

With regard to claim 47, Rabenko et al. has a second controller 150 that controls storage of data from the signal processing subsystem using an optimal pattern which allows simultaneous access to data by the FFT subsystem while avoiding collisions among the accessed data (col. 13, lines 9-12). It would have been obvious to modify Falk et al. and Rabenko et al. as applied to claim 43 by using a first controller as taught in Rabenko et al. in order to store data more efficiently.

With regard to claim 48, Rabenko et al. is an electronic system which includes one of cellular telephones, portable communications devices and portable computing devices (abstract). It would have been obvious to modify Falk et al. and Rabenko et al. as applied to claim 43 by use with the suggested devices of Rabenko et al. in order to provide a platform for the present invention.

With regard to claim 49, Rabenko et al. recites a serial interface between the signal processing system and the input sample system (col. 13, lines 38-55). It would have been obvious to modify Falk et al. and Rabenko et al. as applied to claim 43 by using a serial interface as suggested in Rabenko et al. in order to take advantage of this well known technology.

Claim 5 is rejected on the ground of nonstatutory obviousness-type double patenting over Rabenko et al. and Falk et al. as applied to claim 1 in view of Kanack et al. (US Pat 6263034).

With regard to claim 5, Rabenko et al. have the at least one configurable parameter of the matched filter being the number of taps (col. 66, lines 55-62) as does Kanack et al. which also shows the number of accumulations and a tap offset (col. 8, line 44 - col. 9, line 2). It would have been obvious to modify Rabenko et al. and Falk et al. by adding the filter control parameters of Kanack et al. in order to reduce “jitter” in a digital processing system.

Claims 7 and 20 are rejected on the ground of nonstatutory obviousness-type double patenting over Rabenko et al. and Falk et al. as applied to claim 1 in view of Sih et al. (US Pat 6480529).

With regard to claim 7, Sih et al. teach feeding the output of a matched filter to a coherent accumulator (col. 4, lines 1-10). It would have been obvious to modify Falk et al. and Rabenko et al. to provide the matched filter output to a coherent accumulator in order to provide a fast and flexible and efficient system.

With regard to claim 20, Sih et al. teach the ability to use both the IS-95 system and a GPS system (Abstract). It would have been obvious to modify Rabenko et al. to handle a both satellite system and a terrestrial system as taught in Sih et al. in order to provide positioning service using two sources for robust operation.

Claims 16 and 23 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 2 of Falk et al. (U.S. Pat 7639180) in view of Rabenko et al.

With regard to claim 16, the discussion above regarding Falk et al. and Rabenko et al. as applied to claim 1 is incorporated herein. With specific regard to claim 16, Falk et al. teach feeding data from an FFT system to a non-coherent accumulator (noncoherent summation, col. 21, lines 2-3). It would have been obvious to modify Falk and Rabenko et al. as applied to claim 1 to provide a non-coherent accumulator in order to provide a fast and flexible and efficient system.

With regard to claim 23, the discussion above regarding Falk et al. and Rabenko et al. as applied to claim 1 is incorporated herein. With specific regard to claim 23, the memory subsystem of Falk et al. is configurable into regions that include an input sample memory (Falk et al., col. 20, line 67 – col. 21, line 1) and teach storage of coherent data in a coherent memory (Falk et al., col. 21, line 1) and an noncoherent summation that stores noncoherent data (Falk et al., col. 21, lines 2-3). It would have been obvious to modify Rabenko et al. and Falk et al., as applied to claim 1 by configuring the memory into regions as taught in both Rabenko et al. and Falk et al. to store input samples, coherent data and incoherent data in order to provide an organizational structure to said data and samples.

Claims 21 and 45 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 16 of Falk et al. (U.S. Pat 7639180) in view of Rabenko et al.

With regard to claim 21, the discussion above regarding Falk et al. and Rabenko et al. as applied to claim 1 is incorporated herein. With specific regard to claim 21, Falk

et al. show that it has long been known that GPS includes operational modes including a wide, low resolution search (col. 23, lines 4-5), a narrow, high precision search (col. 23, lines 6-7) and a tracking mode (col. 23, lines 8-9). It would have been obvious to modify Rabenko et al. and Falk et al. as applied to claim 1 by using the operational modes of Falk et al. in order to provide an operational framework for position determination.

With regard to claim 45, in Rebenko et al. the signal processing system includes an input sample subsystem 736 that receives data via at least one channel and produces input data samples (col. 44, lines 45-47). Falk et al. teaches a signal processing system being configurable to process satellite signal data in a satellite based positioning system (col. 20, lines 47-48t). Falk et al. show that it has long been known that GPS includes operational modes including a wide, low resolution search (cold start, col. 1, lines 41-58), a narrow, high precision search (hot start, col. 2, lines 8-28) and a tracking mode (col. 23, lines 4-12). It would have been obvious to modify Falk et al. and Rebenko et al. as applied to claim 43 by using the system with GPS and using the modes in order to provide robust operation to the GPS locating service.

Claim 22 is rejected on the ground of nonstatutory obviousness-type double patenting over Rabenko et al. and Falk et al. as applied to claim 1 in view of Schuchman et al.

With regard to claim 22, Schuchman et al. show that it has long been known that GPS includes operational modes including a cold start (col. 1, lines 41-58), a coarse

acquisition mode (warm start, col. 1, line 59 – col. 2, line 7), a hot start (col. 2, lines 8-28) and a tracking mode (col. 2, lines 29-41). It would have been obvious to modify Rabenko et al. and Falk et al. as applied to claim 1 by using Schuchman's operational modes in order to provide an operational framework for position determination.

Claim 24 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 3 of Falk et al. (U.S. Pat 7639180) in view of Rabenko et al.

With regard to claim 24, the discussion above regarding Falk et al. and Rabenko et al. as applied to claim 1 is incorporated herein. With specific regard to claim 24, Falk et al. show that GPS includes operational modes including a cold start (col. 21, line 5). Falk et al. have the memory subsystem configured into regions (col. 20, lines 60-61) that include an input sample memory (Falk et al., col, 20, line 67) and a noncoherent summation that stores incoherent data (col. 20, lines 2-3) where the input sample memory is significantly greater than the NCS memory (col. 21, lines 8-9). In Rabenko et al., the input sample memory is filled with input data samples in a one-shot manner such that the signal processing subsystem processes data in the filled input sample memory at least once before the data is overwritten (Rabenko et al., Fig. 4, col. 13, lines 6-27). It would have been obvious to modify Rabenko et al. and Falk et al. as applied to claims 1 and 2 by using the operational modes and configuring the memory into regions as taught in both Rabenko et al. and Falk et al. to store input samples and incoherent data in order to provide an organizational structure to said data and samples.

Claim 25 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 4 of Falk et al. in view of Rabenko et al.

With regard to claim 25, the discussion above regarding Falk et al. and Rabenko et al. as applied to claim 24 is incorporated herein. With specific regard to claim 25, in Falk et al. the signal processing unit produces coherent data which is transmitted to an FFT subsystem (col. 21, lines 16-17) which produces noncoherent data and stores same in the NCS memory (Falk et al., col. 21, lines 17-19). It would have been obvious to modify Rabenko et al. and Falk et al as applied to claim 24 by directing coherent and noncoherent data to two locations in order to avoid mathematical conundrums by improper usage of same

Claim 26 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 6 of Falk et al. (U.S. Pat 7639180) in view of Rabenko et al.

With regard to claim 26, the discussion above regarding Falk et al. and Rabenko et al. as applied to claim 1 is incorporated herein. With specific regard to claim 26, Falk et al. show a coarse acquisition mode (col. 21, line 30) and have the memory subsystem configured into regions (col. 21, line 31) that include an input sample memory, a coherent memory and a noncoherent summation that stores incoherent data (col. 21, lines 31-32). In Falk et al., the NCS memory is significantly greater than either the coherent memory or the input sample memory (col. 21, lines 34-35) and the input

sample memory is filled with input data samples in a cyclic manner such that the signal processing subsystem reads out data from one area while the input sample subsystem writes data to another area (col. 21, lines 37-41). It would have been obvious to modify Rabenko et al. and Falk et al. as applied to claim 1 by using the operational modes and configuring the memory into regions as taught in Falk et al. to store input samples, coherent data and incoherent data in order to provide an organizational structure to said data and samples.

Claim 27 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 7 of Falk et al. in view of Rabenko et al.

With regard to claim 27, the discussion above regarding Falk et al. and Rabenko et al. as applied to claim 24 is incorporated herein. With specific regard to claim 27, in Falk et al. the signal processing unit produces coherent data which is stored in the coherent memory (col. 21, lines 44-45) which is moved to the FFTsubsystem (col. 21, lines 45-46). It would have been obvious to modify Rabenko et al. and Falk et al. as applied to claim 26 by directing coherent data to coherent memory and FFT in order to provide the proper data to a coherent process.

Claim 28 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 10 of Falk et al. (U.S. Pat 7639180) in view of Rabenko et al.

With regard to claim 28, the discussion above regarding Falk et al. and Rabenko et al. as applied to claim 1 is incorporated herein. With specific regard to claim 28, Falk et al. show a hot start (col. 21, line 60) and have the memory subsystem configured into regions that include an input sample memory, a coherent memory and an NCS memory that stores incoherent data (col. 21, lines 61-62). The NCS memory is significantly greater that either the input sample memory or the coherent memory (col. 21, lines 63-64). In Falk et al., the input sample memory is filled with input data samples in a cyclic manner such that the signal processing subsystem reads out data from one area while the input sample subsystem writes data to another area (Falk et al., col. 21, line 65 - col. 22, line 2). In Falk et al. the signal processing unit produces coherent data which is stored in the coherent memory (col. 22, lines 3-4) which is configured to include a scratch area and a plurality of coherent areas, each for storage of coherent data from a satellite (Falk et al., col. 22, lines 5-7). It would have been obvious to modify Rabenko et al. and Falk et al. as applied to claim 1 by using the operational modes and configuring the memory into regions as taught in both Rabenko et al. and Falk et al. to store input samples, coherent data and incoherent data in order to provide an organizational structure to said data and samples.

Claim 29 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 11 of Falk et al. in view of Rabenko et al.

With regard to claim 29, the discussion above regarding Falk et al. and Rabenko et al. as applied to claim 28 is incorporated herein. With specific regard to claim 29, in

Falk et al. the signal processing unit produces coherent data which is stored in the coherent memory (col. 22, lines 9-10) which is moved to an FFT subsystem (col. 22, lines 10-11). It would have been obvious to modify Rabenko et al. and Falk et al. as applied to claim 28 by directing coherent data to coherent memory and FFT in order to provide the proper data to a coherent process.

Claim 30 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 14 of Falk et al. (U.S. Pat 7639180) in view of Rabenko et al.

With regard to claim 30, the discussion above regarding Falk et al. and Rabenko et al. as applied to claim 1 is incorporated herein. With specific regard to claim 30, Falk et al. show a tracking mode (col. 22, lines 23), Falk et al. have the memory subsystem configured into regions that include an input sample memory, a coherent memory and an NCS memory (col. 22, lines 24-25). The NCS memory is of significantly greater size than either of the input sample memory or the coherent memory (col. 22, lines 26-27). The input sample memory is filled with input data samples in a cyclic manner such that the signal processing subsystem reads out data from one area while the input sample subsystem writes data to another area (col. 22, lines 28-32). The signal processing unit produces coherent data which is stored in the coherent memory (col. 22, lines 33-34) which is configured to include a scratch area and a plurality of coherent areas, each for storage of coherent data from a satellite (col. 22, lines 35-37). The coherent data is read to an FFT subsystem (col. 22, line 38). The FFT subsystem produces

noncoherent data and stores same in the NCS memory (col. 22, lines 39-40). A memory subsystem such as the NCS memory is configured into regions (col. 22, lines 40-43). It would have been obvious to modify Rabenko et al. and Falk et al. as applied to claim 1 by using the operational modes and by configuring the memory into regions as taught in Falk et al. to store input samples, coherent data and incoherent data in order to provide an organizational structure to said data and samples.

Claims 32-34, 36-39, 42 and 44 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of Falk et al. (U.S. Pat 7639180) in view of Rabenko et al. and further in view of Williams.

With regard to claim 32, Falk et al. have an electronic system (col. 20, line 45, Rabenko et al., network gateway, Abstract) comprising at least one processor (CPU, Falk et al., col. 20, line 46; Rebenko et al., col. 9, lines 31-35) and a signal processing system coupled to operate under a plurality of operational modes (Falk et al., col. 20, lines 59-60; Rebenko et al., col. 45, lines 58-61). The signal processing system includes a signal processing subsystem that is automatically and dynamically configurable in response with the operational modes (Rebenko et al., col. 9, lines 43-45; col. 46, line 60 – col. 47, line 2; col. 47, lines 20-32). The signal processing system further includes an FFT subsystem that is automatically and dynamically configurable in response to the operational modes (Rebenko et al., col. 63, lines 33-35). The signal processing subsystem further includes at least one matched filter having at least one configurable parameter automatically configured in accordance with the operational

modes (Rebenko et al., col. 9, lines 43-45; col. 46, line 60 – col. 47, line 2; col. 47, lines 20-32). Williams teaches that it is well known that FFT subsystems have at least one of a number of inputs (Williams, col. 9, lines 28-31) and the transform size is automatically configured in accordance with operational modes (Williams, col. 9, lines 42-45). It would have been obvious to modify Rabenko et al. and Falk et al. by using the automatically configured FFT transform as taught in Williams in order to take advantage of the properties of this well known mathematical technique.

With regard to claim 33, the signal processing system includes an input sample subsystem (Falk et al., col. 20, 50-51) that receives data (Falk et al., col. 20, line 8) via at least one channel (Rabenko et al., col. 44, lines 45-47) and produces input data samples (Falk et al, col. 20, line 53).It would have been obvious to modify Falk et al, Rabenko et al. and Williams as applied to claim 32 in order to control data input to the system.

With regard to claim 34, a memory subsystem (memory device, Falk et al., col. 20, line 58) is automatically configurable into a plurality of configurations according to the operational modes (Rabenko et al., col. 44, lines 52-53) . Falk et al. and Rabenko et al. have the memory subsystem configured into regions (Falk et al., col. 20, line 17; Rabenko et al., partitions) each being accessed by a plurality of manners (descriptors) (partitions, col. 13, lines 6-9) wherein each region is accessed by particular subsystems (Falk et al, col. 20, lines 18-19; Rabenko et al., col. 13, lines 19-23) wherein one of the regions stores data words from the processor (Falk et al., col. 20, lines 19-20) that determines the configuration of the memory subsystem including sizes of the regions

and manners of access (Falk et al., col 20, line 21; Rabenko et al., col. 13, lines 15-18). It would have been obvious to modify Falk et al., Rabenko et al. and Williams as applied to claim 32 by using the memory subsystems of Falk et al. and Rabenko et al. in order to organize incoming data for use by the other subsystems.

With regard to claim 36, Rabenko et al. further describe at least one sequencer (DOSCIS) coupled to the processor that automatically and dynamically controls time multiplexed use of at least one of the signal processing subsystem and the FFT subsystem (col. 6, lines 52-62; col. 17, lines 30-48) by controlling channel access to at least one of the signal processing subsystem and the FFT subsystem in accordance with at least one rule (col. 6, lines 52-62; col. 17, lines 30-48). In Rabenko et al., the sequencer automatically configures at least one of the signal processing subsystem and the FFT subsystem using information from the at least one memory area (col. 18, line 62- col. 19, line 12). It would have been obvious to modify Falk et al, Rabenko et al. and Williams as applied to claim 32 by providing a sequencer as taught in Rabenko et al. in order to process data more efficiently.

With regard to claim 37, Rabenko et al. has a first controller 150 that controls storage of data from the signal processing subsystem using an optimal pattern which allows simultaneous access by the FFT subsystem while avoiding collisions among the accessed data (col. 13, lines 9-12). It would have been obvious to modify Falk et al, Rabenko et al. and Williams as applied to claim 32 by providing a first controller in order to control the flow of data within the system.

With regard to claim 38, Rabenko et al. further comprise at least one second controller 112 coupled among the signal processing subsystem, the FFT subsystem and the memory subsystem (col. 10, lines 38-65) which controls transfer of data among the signal processing system and the FFT subsystem (col. 10, lines 38-65). It would have been obvious to modify Falk et al., Rabenko et al. and Williams as applied to claim 32 by providing a second controller in order to control the flow of data within the system.

With regard to claim 39, Falk et al. teach a signal processing system being configurable to process satellite signal data in a satellite based positioning system (col. 20, line 47-49). It would have been obvious to modify Falk et al., Rabenko et al. and Williams as applied to claim 32 to handle a satellite system as taught in Falk et al. in order to provide high performance and robust operation of the present invention to a positioning system.

With regard to claim 42, Rabenko et al. is an electronic system which includes one of cellular telephones, portable telephones, portable communications devices, personal computers, portable computing devices and personal digital assistants (abstract). It would have been obvious to modify Falk et al., Rabenko et al. and Williams as applied to claim 32 by using with various devices in order to provide access to networks for such devices.

With regard to claim 44, in Rabenko et al. the signal processing subsystem further includes at least one matched filter having at least one configurable parameter automatically configured in accordance with the operational modes (col. 9, lines 43-45; col. 46, line 60 – col. 47, line 2; col. 47, lines 20-32). Williams teaches that it is well

known that FFT subsystems have at least one of a number of inputs (col. 9, lines 28-31) and the transform size is automatically configured in accordance with operational modes (col. 9, lines 42-45). It would have been obvious to modify Falk et al., Rabenko et al. as applied to claim 43 by using the automatically configured FFT transform as taught in Williams in order to take advantage of the properties of this well known mathematical technique.

Claim 35 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Falk et al., Rabenko et al. and Williams as applied to claim 32 further in view of Kanack et al.

With regard to claim 35, Rabenko et al. have the at least one configurable parameter of the matched filter being the number of taps (col. 66, lines 55-62) as does Kanack et al. which also shows the number of accumulations and a tap offset (col. 8, line 44 - col. 9, line 2). It would have been obvious to modify Rabenko et al. and Williams by adding the filter control parameters of Kanack et al. in order to reduce “jitter” in a digital processing system.

Claim 40 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 16 of Falk et al. (U.S. Pat 7639180) in view of Rabenko et al.

With regard to claim 40, the discussion above regarding Falk et al. and Rabenko et al. as applied to claim 32 is incorporated herein. With specific regard to claim 40,

Falk et al. show that it has long been known that GPS includes operational modes including a wide, low resolution search (col. 23, lines 4-5), a narrow, high precision search (col. 23, lines 6-7) and a tracking mode (col. 23, lines 8-9). It would have been obvious to modify Rabenko et al. and Falk et al. as applied to claim 32 by using the operational modes of Falk et al. in order to provide an operational framework for position determination.

Claim 41 is rejected on the ground of nonstatutory obviousness-type double patenting) as being unpatentable over Falk et al., Rabenko et al. and Williams as applied to claim 32 further in view of Schuchman et al.

With regard to claim 41, Schuchman et al. show that it has long been known that GPS includes operational modes including a cold start (col. 1, lines 41-58), a coarse acquisition mode (warm start, col. 1, line 59 – col. 2, line 7), a hot start (col. 2, lines 8-28) and a tracking mode (col. 2, lines 29-41). It would have been obvious to modify Falk et al., Rabenko et al. and Williams as applied to claim 32 by using Schuchman's operational modes in order to provide an operational framework for position determination.

Claim 50 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Falk et al. and Rabenko et al. as applied to claim 1 further in view of Horton (US Pat 6421696).

With regard to claim 50, Horton shows that twiddle factors or algorithms are well known techniques used in connection with fast Fourier transforms. It would have obvious to modify Rabenko et al. as applied to claim 1 by using twiddle factors as taught in Horton in order to take advantage of these well known mathematical techniques.

Claim 51 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 27 of Falk et al. (U.S. Pat 7639180) in view of Rabenko et al.

With regard to claim 51, both Falk et al, and Rabenko et al. have an electronic system (Falk et al., col. 24, line 17; Rabenko et al., network gateway, Abstract) comprising means for controlling processing (processing means, Falk et al, col. 24, line 18; Rabenko et al., col. 9, lines 31-35) and means for processing signals coupled to the means for controlling processing 160 (signal processing system, Falk et al., col. 24, line 19, Rabenko et al., col. 36, line 65 – col. 37, line 4). The means for processing signals operates in accordance with operational modes of the system (Rabenko et al., col. 45, lines 58-61). The means for processing includes means for receiving data and producing input data samples (input sample means, Falk et al, col. 24, lines 23-26) that receives data via at least one channel and produces input data samples (Rabenko et al., col. 44, lines 45-47). Means for generating coherent data (first signal processing means, Falk et al, col. 24, lines 27-28) using the input data samples includes at least one matched filter means having at least one configurable parameter automatically configured in accordance with the operational modes (Rabenko et al., col. 9, lines 43-

45; col. 46, line 60 – col. 47, line 2; col. 47, lines 20-32). Means for generating FFTs (second signal processing means, Falk et al., col. 24, lines 29-30) has a number of inputs and a transform size automatically configured in accordance with the operational modes (Rabenko et al., col. 63, lines 33-35). Means for storing data is automatically configurable into a plurality of configurations according to the operational modes (memory device, Falk et al., col. 24, lines 31-38); Rabenko et al. col. 44, lines 52-53). It would have been obvious to modify Falk et al. as taught in Rabenko et al. in order to speed up calculations by organizing the memory subsystem to operate efficiently under different conditions.

Pertinent Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ammar et al. (US Pat 5831570) improves the resolution of targets in a monopulse radar beam.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FRANK MCGUE whose telephone number is (571)270-5987. The examiner can normally be reached on 8:30am to 5:00pm Eastern, Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Tarcza can be reached on (571)272-6032. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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